MEMORY DEVICE ARRAY HAVING A PAIR OF MAGNETIC BITS SHARING A COMMON CONDUCTOR LINE

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BACKGROUND OF THE INVENTION

The present invention pertains to the field of resistive memory cell arrays. More particularly, this invention relates to a memory array having memory bit pairs sharing a common conductor to increase array density.

A resistive random access memory (RAM) is a cross point type memory array of a planar matrix of spaced memory cells sandwiched between two meshes of conductors running in orthogonal directions above and below the cells. An example is the resistive RAM array 10 shown in Figure 1. The row conductors 12 running in one direction are referred to as the word lines, and the column conductors 14 extending in a second direction usually perpendicular to the first direction are referred to as the bit lines. The memory cells 16 are usually arranged in a square or rectangular array so that each memory cell unit 16 is connected with one word line 12 and an intersecting bit line 14.

In a resistive RAM array, the resistance of each memory cell has more than one state, and the data in the memory cell is a function of the resistive state of the cell. The resistive memory cells may include one or more magnetic layers, a fuse or anti-fuse, or any element that stores or generates information by affecting the magnitude of the nominal resistance of the element. Other types of resistive elements used in a resistive RAM array include poly-silicon resistors as part of a read-only memory, or phase charge material as rewritable memory device.

One type of resistive random access memory is a magnetic random access memory (MRAM), in which each memory cell is formed of a plurality of magnetic layers separated by insulating layers. One magnetic layer is called a pinned layer, in which the magnetic orientation is fixed so as not to rotate in the presence of an applied magnetic field in the range of interest. Another magnetic layer is referred to as a sense layer, in which the magnetic orientation is variable between a state aligned with the state of the pinned layer and a state in misalignment with the state of the pinned layer. An insulating tunnel barrier layer sandwiches between the magnetic pinned layer and the magnetic sense layer. This insulating tunnel barrier layer allows quantum mechanical tunneling to occur between the sense layer and the pinned layer. The tunneling is electron spin dependent, causing the resistance of the memory cell, a